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Attorney Docket: MXIC 1553-3

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Ann Jonsson
Ann Jonsson

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Chih C. YEH et al.

Application No. 10/642,249

Confirmation No.: 1545

Filed: 15 August 2003

Title: **Method for Programming
Programmable Eraseless Memory**

*Group Art Unit: 2818**Examiner: Unassigned***Customer No. 22470****FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Enclosed with this statement is Form PTO/SB/O8A. The Examiner is requested to initial the form and return it to the undersigned in accordance with M.P.E.P. 609.

Also enclosed with this statement is a copy of each cited document as required by 37 C.F.R. 1.98. The exception to this, in accordance with the 05 August 2003 Official Gazette Notice in which the USPTO waives the requirement for submitting copies of U.S. Patent and Publications for cases filed after 30 June 2003, is that copies of U.S. Patent documents and copies of U.S. Patent publications are not being submitted.

This statement should be considered under 37 C.F.R. 1.97(b) because it is being filed before the mailing date of the first Office Action on the merits.

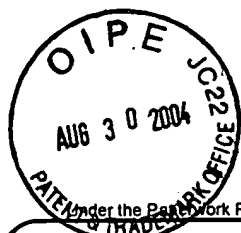
Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (MXIC 1553-3). A duplicate copy of this authorization is enclosed.

Respectfully submitted,

Date: 26 Aug 2004

By: 
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PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	10/642,249
Filing Date	15 August 2003
First Named Inventor	Chih C. Yeh et al.
Art Unit	2818
Examiner Name	Unassigned
Attorney Docket Number	MXIC 1553-3

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	A1	US- 6,650,143	11-18-2003	Peng	
	A2	US- 6,667,902	12-23-2003	Peng	
	A3	US- 6,671,040	12-30-2003	Fong et al.	
	A4	US- 6,700,151	03-02-2004	Peng	
	A5	US- 2002/0094611	07-17-2002	Wu et al.	
	A6	US- 2004/0008538	01-15-2004	Peng	
	A7	US- 2004/0047218	03-11-2004	Peng	
	A8	US- 2004/0106251	06-03-2004	Forbes et al.	
	A9	US- 2004/0129995	07-08-2004	Yeo et al.	
	A10	US- 2004/0137688	07-15-2004	Chang et al.	
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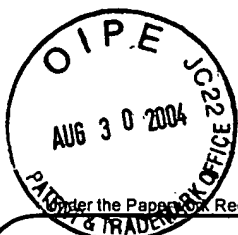
FOREIGN PATENT DOCUMENTS						
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		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

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STATEMENT BY APPLICANT**

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Application Number 10/642,249

Filing Date 15 August 2003

First Named Inventor Chih C. Yeh et al.

Art Unit 2818

Examiner Name Unassigned

Sheet 2 of 2

Attorney Docket Number MXIC 1553-3

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C1	Stathis, J.H., "Reliability Limits for the Gate Insulator in CMOS Technology" IBM. J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, 265-286	
	C2	Miranda, Enrique, et al. "Analytic Modeling of Leakage Current Through Multiple Breakdown Paths in SiO ₂ Films" IEEE 39th Annual IRPS 2001, 367-379	
	C3	Wu, E.Y. et al., "Voltage-Dependent Voltage-Acceleration of Oxide Breakdown for Ultra-Thin Oxides" Electron Devices Meeting, 2000, IEDM Technical Digest International, 10-13 December 2000, 541-544	
	C4	Sune, Jordi et al. "Post Soft Breakdown Conduction in SiO ₂ Gate Oxides" Electron Devices Meeting, 2000 IEDM Technical Digest International, 10-13 Dec. 2000 533-536	
	C5	Rasras, Mahmoud et al. "Substrate Hole Current Origin After Oxide Breakdown" Electron Devices Meeting, 2000 IEDM Technical Digest International, 10-13 Dec. 2000, 537-540	
	C6	Lombardo, S., et al. "Softening of Breakdown in Ultra-Thin Gate Oxide nMOSFETs at Low Inversion Layer Density" Reliability Physics Symposium 2001, Proceedings 39th Annual 2001 IEEE International, 30 April, 3 May 2001, 163-167	
	C7	Monsieur, F., et al. "A Thorough Investigation of Progressive Breakdown in Ultra-Thin Oxides Physical Understanding and Application for Industrial Reliability Assessment", Reliability Physics Symposium Proceedings 2002, 40th Annual 7-11 April 2000, 45-54	
	C8	Suehle, J. "Ultra-Thin Gate Oxide Reliability and Implications for Qualification, Design and Use in Ionizing Radiation Environments" NASA Microelectronics Reliability and Qualification Workshop, Manhattan Beach Marriott, Manhattan Beach, CA 12/3/02 30 pgs	

Examiner Signature	Date Considered
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